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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,274	12/04/2003	Barry J. Oldfield	10001491-4	7124

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EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,274	OLDFIELD ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,12-25 and 35* is/are rejected.

7)☒ Claim(s) *3-11 and 26-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/4/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/4/03; 9/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims (15 & 19) and 16-18 are rejected under the judicially created doctrine of double patenting over claims 1, and 2-4 of U. S. Patent No. 6,687,872, respectively, since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

"A method of calculating parity segments comprising:

providing a parity calculation module configured to calculate one or more parity segments,

with the parity calculation module:

receiving one or more data segments that are to be used to calculate one or more parity segments;

receiving one or more parity coefficients that are to be used to

calculate the one or more parity segments;

operating on the one or more data segments and the one or more parity coefficients to provide an intermediate computation result,

writing the intermediate computation result to one or more local buffers, and

within one clock cycle of an associated clock, receiving (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operating on them to provide a result that is stored in the one or more local buffers";

"Wherein the parity calculation module comprises one or more local memory components configured to locally hold data that is used in the calculation of the parity segment";

"the parity calculation module comprise an application specific integrated circuit (ASIC)";

"one or more local buffers comprises SRAMs"; and

"wherein the parity calculation module comprises an application specific integrated circuit (ASIC), and the one or more local buffers comprise SRAMs on the ASIC".

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

3. Claims (1 & 2) and 12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of U.S. Patent No. 6,687,872, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent substantially teaches the claimed invention. The patent does not explicitly teach that coefficients are chosen from a plurality of coefficient subsets, each the coefficient subset is classified based on a respective parity operation. However, it would have been obvious to one skilled in the art at the time the invention was made to realize that each coefficient would have been formed and chosen based on a respective parity operation. One having ordinary skill in the art would be motivated to realize so because the use of parity operation for generating coefficients are well-known in the art.

4. Claims 20 and 21-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 7 and 8-10 of U.S. Patent No. 6,687,872, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent substantially teaches the claimed invention. The patent does not explicitly teach that coefficients are chosen from a plurality of coefficient subsets, each the coefficient subset is classified based on a respective parity operation. However, it would have been obvious to one skilled in the art at the time the invention was made to realize that each coefficient would have been formed and chosen based on a respective parity operation. One having ordinary skill in the art would be motivated to realize so because the use of parity operation for generating coefficients are well-known in the art.

5. Claims (24 & 25) and 35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of U.S. Patent No. 6,687,872, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent substantially teaches the claimed invention. The patent does not explicitly teach that parity coefficients are chosen from a plurality of coefficient subsets, each the coefficient subset is classified based on a respective parity operation. However, it would have been obvious to one skilled in the art at the time the invention was made to realize that each parity coefficient would have been formed and chosen based on a respective parity operation. One having ordinary skill in the art would be motivated to realize so because the use of parity operation for generating parity coefficients are well-known in the art.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over George et al. (4,996,690 and George hereinafter).

Claims 13-15:

George discloses the invention substantially as claimed. George shows a communication system (8) (figures 1, 2 & 3) comprising a parity digital generator (18) and a parity memory (16) (figure 1). The parity digital generator (18) calculates parity digits after receiving each byte of data from a buffer memory (24). Then such calculated parity digits are stored into the parity memory (16) via a parity memory interface (78) (figures 2, 5, & 6; column 10 lines 27-68). In the calculate parity digit method (figure 6), a variable for feedback ("FDBK") is set equal to the incoming data byte at parity (data, i) and XORed with previously calculated parity digital represented a parity (PARBLK, i). The notation parity (PARBLK, i) represents an index into the parity memory (16) to the previously stored parity blocks. Then j is increment that the parity digit calculation is repeated (steps 148, 140 & 144) (column 12 line 14-column 13 line 4).

George does not explicitly teach that writing the intermediate computation result to one or more local buffers. However, it would have been a matter of design choice whether or not to temporarily stored the intermediate computation result into buffer(s). Such a choice would depend on the willingness of buffers' expense because the intermediate computation result is read out shortly for the next computation result.

Claim 16:

George does not explicitly disclose the ASIC. George, however, teach the parity digital generator (18) is suitable to be designed in software or hardware such that an encoder (72) therein can perform equivalent steps for calculating ECC parity digitals (column 8 lines 43-53).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that George's parity digital generator (18) would have been embodied as an ASIC. The artisan would have been motivated to do so because George teaches that such a parity digital generator (18) can be programmed by software (column 8 lines 43-52).

Claim 17:

George's bytes of data are stored in the buffer memory (24) (steps 120) (figure 5, column 10 liens 35-38).

Claim 18:

Claim 18 is rejected for reasons similar to those set forth against claims 16 & 17.

Claim 19:

George's buffer memory (24) holds bytes of data to be used for parity generation (figures 2 & 5, column 10 lines 27-46).

Response to Arguments

9. Applicant's arguments filed 12/4/2004 have been fully considered but they are not fully persuasive.

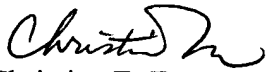
For claims 1-12 and 20-34, examiner agree with applicant's remark that George does not teach a method in which one or more parity coefficients are received that are to be used to calculate the one or more parity segments, such one or more parity coefficients are chosen from a plurality of coefficient subsets, and each of the coefficient subsets is classified based on a respective parity operation. Therefore, art rejection is withdrawn for these claims.

For claims 15-19, applicant argues that George does not teach a method of which within one clock cycle of an associated clock, receives (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operates on them to provide a result that is stored in the one or more local buffers. Examiner however, disagrees to applicant's remark. In George's reference, after incrementing the index j, the processing of parity calculation continues again (column 12 line 56-column 13 line 4). In other words, the receiving of a variable for feedback and a previously calculated parity digital is performed again.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christine T. Tu
Primary Examiner
Art Unit 2133

May 27, 2005